What is claimed is:

1. A driver circuit for a display, the circuit having an input receiving a digital input data having n bits for selecting one of a plurality of voltage levels for driving the circuit, the circuit having an output, a plurality of digital signal lines coupled to the digital input data, a plurality of active regions coupled to a first side of the output, each of the plurality of active regions coupled to a separate voltage level, the circuit further including a plurality of pass transistors at a first subset of locations where the plurality of digital signal lines overlap the plurality of active regions, a plurality of depletion-implanted transistors at a second subset of locations where the plurality of digital signal lines overlap the plurality of active regions, wherein:

the number of the plurality of digital signal lines on the first side of the output is an odd number.

2. The circuit of claim 1, wherein the plurality of digital signal lines are polysilicon lines.

3. The circuit of claim 1, wherein the plurality of active regions is a first plurality of active regions, and further including a second plurality of active regions coupled to a second side of the output, and the number of the plurality of digital signal lines on the second side of the output is an odd number.

4. The circuit of claim 1, wherein the number of the plurality of digital signal lines on the first side of the output is equal to 2n-1.

5. The circuit of claim 3, wherein the number of the plurality of digital signal lines on the second side of the output is equal to 2n-1.

6. The circuit of claim 1, wherein said odd number digital signal lines includes a first digital signal line associated with a first digital bit, a second digital signal associated with a second digital bit, and an inverting digital line associated with the second digital bit.

7. A driver circuit for a display, the circuit having an input receiving a digital input data,having n bits for selecting one of a plurality of voltage levels for driving the circuit, the circuit having an output, a plurality of digital signal lines coupled to the digital input data, a plurality of active regions coupled to a first side of the output, each of the plurality of active regions coupled to a separate voltage level, the circuit further including a plurality of pass transistors at a first subset of locations where the plurality of digital signal lines overlap the plurality of active regions, a plurality of depletion-implanted transistors at a second subset of locations where the plurality of digital signal lines overlap the plurality of active regions, the circuit further including:

a plurality of blocking transistors positioned between the input and selected digital signal lines, with at least one of the digital signal lines being coupled to a gate of each of the blocking transistors for controlling each of the blocking transistors.

8. The circuit of claim 7, wherein the plurality of active regions is a first plurality of active regions, and further including a second plurality of active regions coupled to a second side of the output, and the number of the plurality of digital signal lines on the second side of the output is an odd number.

9. The circuit of claim 7, further including a buffer positioned between the input and each digital signal line, wherein the buffers for the digital signal lines that control the blocking transistors are larger in size than the other buffers.

10. The circuit of claim 7, wherein each blocking transistor is either a NMOS switching gate or a CMOS transfer gate.

11. The circuit of claim 7, wherein the number of the plurality of digital signal lines on the first side of the output is an odd number.

12. The circuit of claim 8, wherein the number of the plurality of digital signal lines on the second side of the output is equal to 2n-1.

13. The circuit of claim 11, wherein the number of the plurality of digital signal lines on the first side of the output is equal to 2n-1.

14. A driver circuit for a display, the circuit having an input receiving a digital input data having n bits for selecting one of a plurality of voltage levels for driving the circuit, the circuit having an output, a plurality of digital signal lines coupled to the digital input data, a plurality of active regions coupled to a first side of the output, each of the plurality of active regions coupled to a separate voltage level, the circuit further including a plurality of pass transistors at a first subset of locations where the plurality of digital signal lines overlap the plurality of active regions, a plurality of depletion-implanted transistors at a second subset of locations where the plurality of digital signal lines overlap the plurality of active regions, wherein:

the number of the plurality of digital signal lines on the first side of the output is equal to 2n-2.

15. The circuit of claim 14, wherein the plurality of digital signal lines are polysilicon lines.

16. The circuit of claim 14, wherein the plurality of active regions is a first plurality of active regions, and further including a second plurality of active regions coupled to a second side of the output, and the number of the plurality of digital signal lines on the second side of the output is equal to 2n-2.

17. The circuit of claim 14, wherein a first of the digital signal lines is discontinued between two adjacent active regions to form a first digital segment carrying the digital signal, and a second digital segment carrying a digital signal that is inverted from the digital signal of the first digital segment.

18. The circuit of claim 16, wherein one of the digital signal lines on the second side is discontinued between two adjacent active regions to form a first digital segment carrying the digital signal, and a second digital segment carrying a digital signal that is inverted from the digital signal of the first digital segment.

19. The circuit of claim 14, further including a plurality of blocking transistors positioned between the input and selected digital signal lines, with at least one of the digital signal lines being coupled to a gate of each of the blocking

27. The circuit of claim 21, wherein a first of the digital signal lines is discontinued between two adjacent active regions to form a first digital segment carrying the digital signal, and a second digital segment carrying a digital signal that is inverted from the digital signal of the first digital segment.

28. The circuit of claim 21, wherein the plurality of active regions is a first plurality of active regions, and further including a second plurality of active regions coupled to a second side of the output.

29. The circuit of claim 28, wherein the number of the plurality of digital signal lines on the second side of the output is equal to 2n-2.

30. The circuit of claim 28, wherein the number of the plurality of digital signal lines on the second side of the output is equal to 2n-1.

31. The circuit of claim 28, wherein one of the digital signal lines on the second side is discontinued between two adjacent active regions to form a first digital segment carrying the digital signal, and a second digital segment carrying a digital signal that is inverted from the digital signal of the first digital segment.

32. The circuit of claim 21, wherein the digital signal line has at least two discontinued segments, with a level shifter coupling between the the discontinued segments.